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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,163	07/28/2003	S. Jauher A. Zaidi	63479.0118	4353

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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,163	ZAIDI ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,7 and 9-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7 and 9-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The amendment filed 3/2/05 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: replacing the statement that "The first internal unidirectional bus controls transactions between the processor subsystem(s) the MAC, and the DMA peripheral(s) using a single centralized address decoder" with "The first internal unidirectional bus controls transactions between the processor subsystem(s) and the DMA peripheral(s) using Memory Access Controller (MAC)". The examiner was unable to find support for this change in the specification.

Applicant is required to cancel the new matter in the reply to this Office Action.

Response to Arguments

2. Applicant's arguments filed 3/2/05 have been fully considered but they are not persuasive.

In regards to applicants arguments regarding the 112, 2nd Paragraph and 101 rejection of claims 9-14: The examiner did not reject these claims over 37 CFR 1.75(c). The rejection does not state that the claims are improper multi dependent claims. The rejection is that "A dependant claim" is not a process, machine, manufacture, or composition of matter, or any new and useful improvement thereof. While "A dependent claim" which is a legal instrument may be useful and

have monetary value "A dependent claim" is not one of the statutory classes of invention set forth under 35 U.S.C. § 101. Further claim 9 which is multi dependent on claims 1, 3, 5 and 7. Is mixing classes of invention. In the case of 9 dependent on 1 or 3 it is mixing "A system-on-Chip" (machine) with "A dependent claim" (legal instrument). In the case of 9 dependent on 5 or 7 it is mixing "A method" (process) with "A dependent claim" (legal instrument). Under 112, 2nd a claim which purports to be both a machine and a legal instrument is ambiguous and therefor does not particularly point out and distinctly claim the subject matter of the invention *Ex parte Lyell* 17 USPQ2d 1548.

In regards to applicants argument that they have been allowed to claim "A dependent claim" before: Just because other examiners did not properly reject applicants improperly claiming "A dependent claim" which is a non-statutory class of invention, does not mean that claiming "A dependent claim" should now be allowed. It is not the prevue of the examiner to address the validity of issued patents. If the applicants wish to address the validity of the patents the applicants referenced the applicant need only file a reissue application including the reason for the reissue application.

In regards to applicants argument that Lambrecht does not limit the communications on its buses, and can support both unidirectional and bidirectional communications: This is correct. Just because Lambrecht teaches more than the applicants does not alleviate that Lambrecht teaches the claimed subject matter. Lambrecht expressly states that bus 230 or 232 may be unidirectional and that bus 230 may be point-to-point as well as showing in figure 4 the bus being a unidirectional point-to-point bus.

3. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that the busses are limited to the components attached to the buses.) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Just because Lambrecht teaches more than the applicants does not alleviate that Lambrecht teaches the claimed subject matter.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In regards to applicants argument that Elabd contains a bus that is similar in structure to applicants second internal bus. But Elabd does not however contain a structure similar to applicants first internal bus. Lambrecht teaches both the first and second internal bus. Elabd teaches a system that on a chip that includes DMA peripheral, a memory access controller which includes a route controller that controls communications between components on the bus, and pipelined memory transactions including out-of-order transactions. The fact that Elabd's bus is a similar structure to applicants claimed second bus is a bonus.

In regards to applicants argument Qureshi does not teach all of the limitations of the claimed invention: The examiner agrees. Qureshi was not applied as a 102 reference.

In regards to applicants arguments regarding Geiger: Since applicants have removed the feature from the claims for which Geiger was applied, Geiger is no longer required and applicants arguments are moot.

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 3, 5, 7, 9-18 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification as originally filed stated that the communication between the

processor subsystems, the memory access controller and the DMA peripherals is done using a single centralized address decoder. The claims currently claim that the communication between the processor subsystems, and the DMA peripherals is done using the memory access controller. This was not in the specification as originally filed.

6. Claims 9-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims which combines description of the single semiconductor integrated circuit with description of method of making/using it violates 35 U.S.C. 112, since the purpose of that paragraph is to require patentee to provide others with notice of boundaries of protection provided by the patent, since a manufacturer or seller at time of making or selling the structure set forth in the claim would have no indication whether it might later be sued for contributory infringement if the structure is later used in accordance with the claimed method. *Ex parte Lyell* 17 USPQ2d 1548.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 9-14 are rejected under 35 U.S.C. 101 because claims which are intended to embrace both product or machine and process is precluded by language of 35 U.S.C. 101, which

sets forth statutory classes of invention in alternative only, and is also invalid under 35 U.S.C. 112, second paragraph, since claim which purports to be both machine and process is ambiguous and therefore does not particularly point out and distinctly claim the subject matter of the invention. *Ex parte Lyell* 17 USPQ2d 1548.

Claims 9-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

While "A dependent claim" may be useful and have monetary value "a dependent claim" is not one of the statutory classes of invention set forth under 35 U.S.C. 101.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-9, 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lambrecht et al PN 5,935,232 in view of Elabd PN 6,526,462.

In regards to claims 1, 3, 5, 7: Lambrecht et al teaches A System-on-chip (SOC) apparatus (100), comprising: a single semiconductor integrated circuit that includes one or more processor subsystems (modules 210 Column 9 lines 17-25); a first internal unidirectional bus that couples to said one or more processor subsystems Figure 2 bus 232 or 230 or alternatively Figure 3 bus 332 or 330), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems (Clock Column 2 lines 14-15).

Lambrecht et al states the modules 210 can be controllers, memories and application specific integrated circuits however Lambrecht et al does not expressly state the modules include DMA peripherals and memory access controllers. Lambrecht et al does not teach pipelined memory transactions including out-of-order transactions. Official notice is taken that signals are only captured on rising edge, falling edge or level sensitive. It would have been obvious to use the rising edge of the clock because this is a common edge to use. Elabd teaches a system on a chip that includes a DMA peripheral (6), memory access controller (30), and pipelined memory transactions including out-of-order transactions (Column 7 line 64 to Column 8 line 14 and Column 9 line 25 to Column 10 line 16) Elabd's Memory access controller includes a route controller that controls the communication between components (Column 1 lines 6-19). It would have been obvious to include Elabd's memory management in the system of Lambrecht et al because this would have increased data processing throughput. Lambrecht et al teaches non-DMA peripherals such as memories and ASIC's a second internal unidirectional bus (230 or 330) that couples said one or more processor subsystems via an interface controller (220) to said non-DMA peripherals, said second internal unidirectional bus has a clock signal (clock) and controls transactions between said one or more processor subsystems, and said non-DMA peripherals) using unidirectional address and transaction control signals.

In regards to claims 9, 15-18 dependant upon any of claims 1, 3: Lambrecht et al teaches said single semiconductor integrated circuit further includes a bus arbiter (350 Column 6 lines 23-30) coupled to said first internal unidirectional bus (332), wherein said arbiter grants access to said first internal unidirectional bus and arbitrates memory accesses for transactions on said first internal unidirectional bus.

In regards to claim 11: Elabd teaches handling Burst read and writes.

In regards to claim 12: Elabd teaches a variable number of clock cycles between pipelined memory transactions (Column 13 line 63 to Column 14 line 8).

In regards to claims 13-14: Lambrecht et al teaches different clock rates on the different buses.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lambrecht et al PN 5,935,232 in view of Elabd PN 6,526,462 as applied to claim 9 above, and further in view of Qureshi et al PN 6,353,867.

In regards to claim 10: Lambrecht et al teaches requests that can be received in any order. Lambrecht et al does not expressly teach memory access arbitration for a selected transaction either overlaps a data transfer associated with a prior transaction. Qureshi et al teaches a System On a Chip that handles on chip split transactions which are memory transactions that overlaps a data transfer associated with prior transactions. It would have been obvious to handle split transactions because this would have prevented waiting of memory accesses that art not ready.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM
May 9, 2005

PAUL R. MYERS
PRIMARY EXAMINER